

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Bernd Deutschmann, et al. Art Unit : Unknown
Serial No. : 10/588,984 Examiner : Unknown
Filed : August 10, 2006 Conf. No. : 4272
Title : CIRCUIT ARRANGEMENT AND METHOD FOR PROTECTING AN
INTEGRATED SEMICONDUCTOR CIRCUIT

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicants request consideration of the references listed on the attached PTO-1449 form. Under 37 C.F.R. § 1.98 (a)(2)(ii), only copies of foreign patent documents and/or non-patent literature are enclosed. Copies of any listed U.S. patents or U.S. patent application publications can be provided upon request.

This statement is being filed within three months of the filing date of the application or before the receipt of a first Office Action on the merits. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: November 1, 2007



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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 14603-026US1	Application No 10/588,984
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant Bernd Deutschmann, et al.	
		Filing Date August 10, 2006	Group Art Unit
(37 CFR §1.98(b))			

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AQ	Examination report for corresponding application EP05707380.1
	AR	Ming-Dou Ker et al "SCR Device with Double-Triggered Technique for On-Chip ESD Protection in Sub-Quarter-Micron Silicided CMOS Processes. IEEE Trans. on Device and Materials Reliability, Vol. 3., No. 3., September 2003; XP 002346581
	AS	
	AT	

Examiner Signature:	Date Considered
EXAMINER: Initials/initials considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	